

FE50MLIR FE50MLNR

DC-50 Fiber Optic LC Transceiver



DESCRIPTION

The Firecomms DC-50 MBd LC transceiver consists of a highly reliable Resonant Cavity Light Emitting Diode (RCLED) with integrated driver IC as a visible optical transmitter and a receiver with a fully integrated photodiode and receiver IC. They are housed in a small form factor housing, compliant with IEC 61754-20. They are capable of sending 50 Mbps digital signals over fiber and operate in the temperature range of -40 °C to +85 °C. The device can operate from 5 V or 3.3 V DC power supply rails.

The transmitter contains a red wavelength RCLED with fully integrated precision driver IC, designed to provide a communication link over POF. The RCLED in this transceiver is a highly reliable visible incoherent light source requiring low operating current. The use of intrinsically eye-safe, visible light simplifies link set-up and testing. The transmitter has a non-inverting optical output.

The receiver is a robust optical to electrical receiver with integrated pulse width distortion minimization circuitry for reliable data transmission. The receiver features a push-pull TTL compatible CMOS output. The receiver is available in inverting and non-inverting options.

AVAILABLE OPTIONS

DC-50 Mb LC Non-Inverting Tx, Inverting Rx	FE50MLIR
DC-50 Mb LC Non-Inverting Tx, Non-Inverting Rx	FE50MLNR



FEATURES

- Reliable LC housing with a “click-lock” connection
- Visible RCLED at red wavelength (650 nm)
- Optimized for data transmission from DC to 50 MBd
- Industrial temperature range -40 °C to +85 °C
- Push Pull TTL Compatible CMOS output
- Dual 5 V and 3.3 V power supply
- RoHS compliant and flame retardant
- (UL 94 V-0) connector housings
- Ultra-low pulse width distortion suitable for burst mode data transmission

APPLICATIONS

Table 2
APPLICATIONS

Application	Automation and Industrial Control, Serial Communications, Voltage Isolation
Standard	Serial RS232, RS485, CAN-Bus, MODBUS, Profibus
Distance	50 meters Step Index POF ^[1]
Speed	DC to 50 MBd

Note: 1. Depending on the installation conditions.

SPECIFICATIONS

Table 3
TRANSCIVER PIN DESCRIPTION

Pin	Name	Symbol
Transmitter		
1	EMI Shield ^[1]	GND
2	Data Input (TTL)	V _{in}
3	Ground	GND
4	Ground	GND
5	V _{cc} (5/3.3 V) ^[2]	V _{cc}
6	V _{cc} (5/3.3 V)	V _{cc}
Receiver		
7	V _{cc} (5/3.3 V)	V _{cc}
8	V _{cc} (5/3.3 V)	V _{cc}
9	Ground	GND
10	Data Output	V _o
11	No Connect	N.C.
12	EMI Shield ^[1]	GND

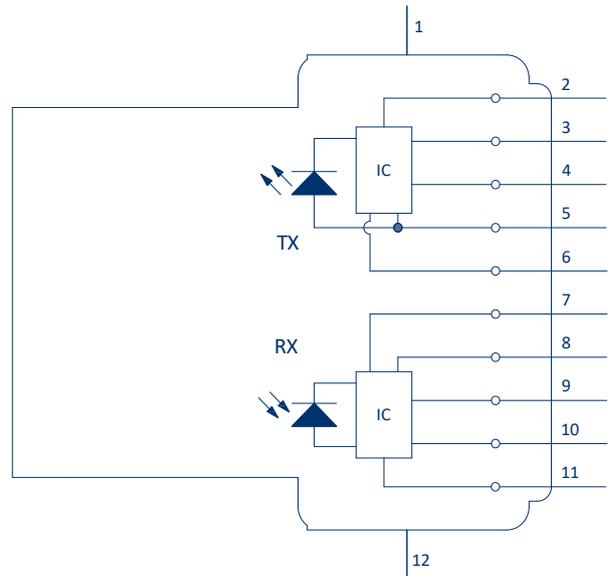


FIGURE 1
Transceiver pin-out, top view

Note:

1. EMI Shield ground pins must be connected to the signal ground plane on the PCB. This is important to prevent cross-talk between Tx and Rx and also to shield the internal fiber optic transceivers (FOTs) from external EMI/EMC and ESD.

2. For reduced power consumption and maximum operating lifetime, it is highly recommended to use a 3.3 V supply.

RECOMMENDED APPLICATION CIRCUIT

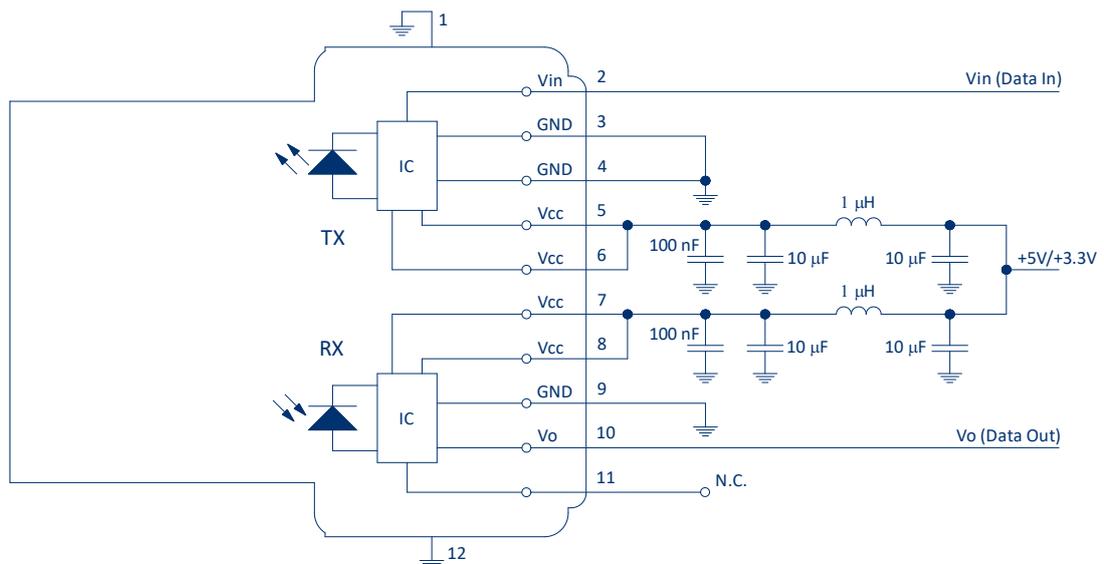


FIGURE 2
Recommended application circuit

GENERAL OPERATION

Inverting Part FE50MLIR

FE50MLIR consists of a non-inverting transmitter and inverting receiver.

Non-Inverting Transmitter

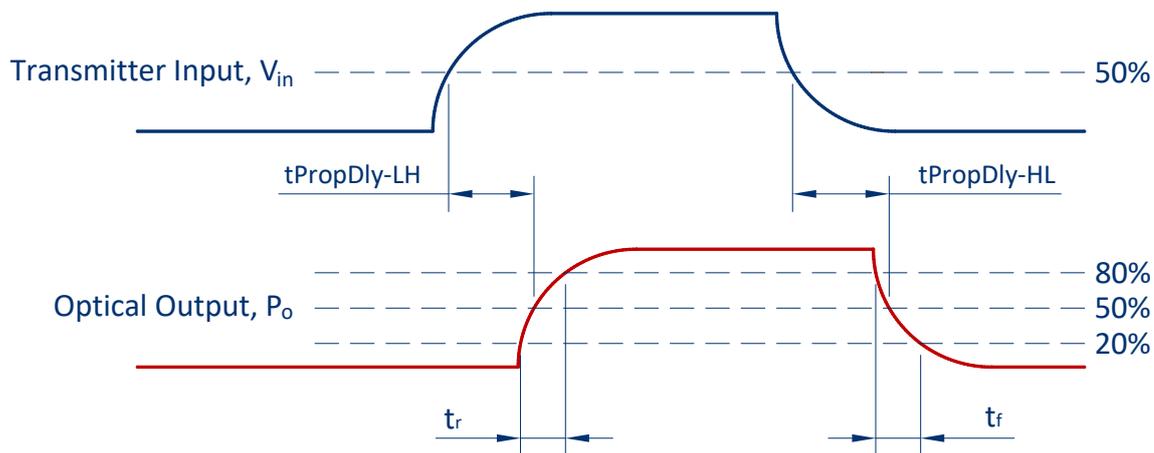


FIGURE 3
FE50MLIR Transmitter Propagation Delay and rise/fall time definitions

Inverting Receiver

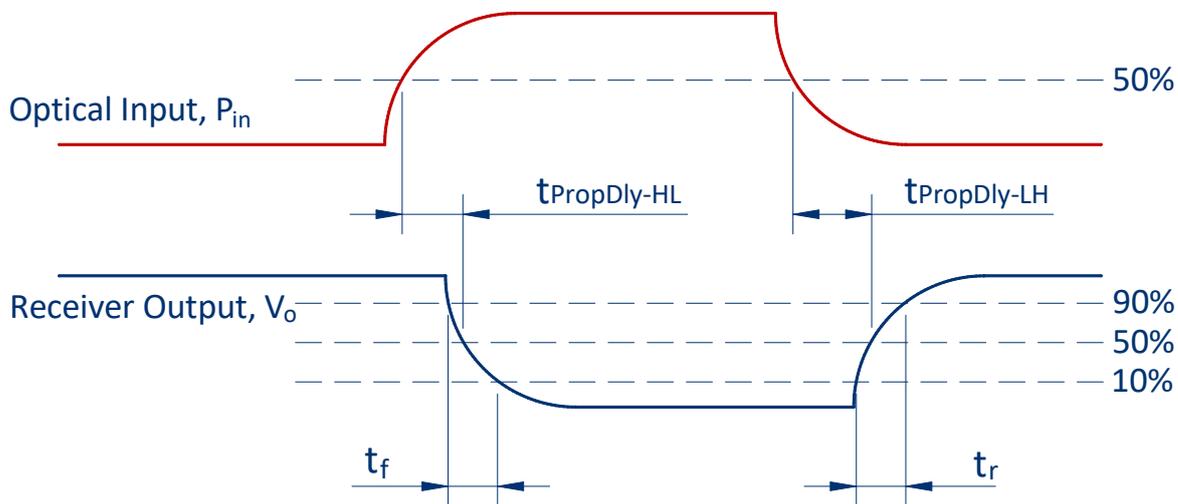


FIGURE 4
FE50MLIR Receiver Propagation Delay and rise/fall time definitions

Inverting Part FE50MLIR (Continued)

FE50MLIR operation during power up, power down or power reset is illustrated below in figures 5, 6 & 7.

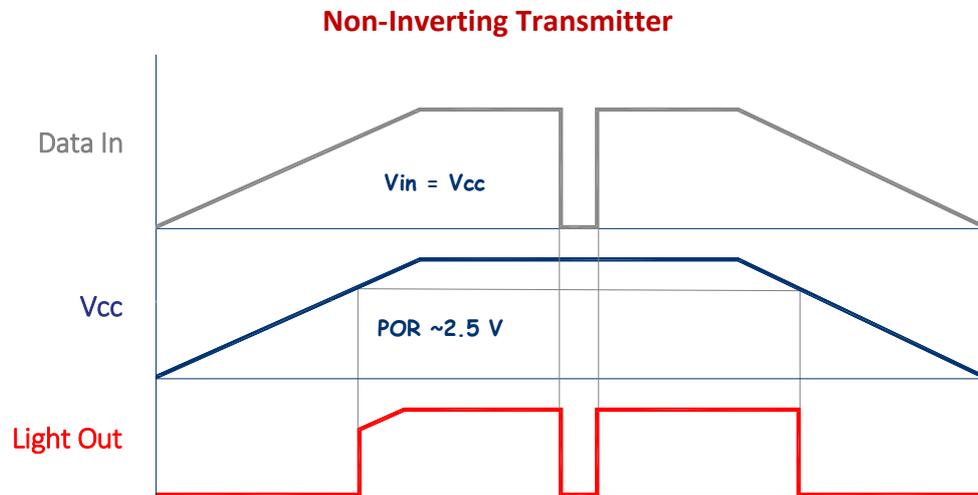


FIGURE 5
FE50MLIR Non-Inverting Tx operation during power cycling with input logic high

During power up as Vcc rises to approximately 2.5 V, there is no light output. Once Vcc reaches 2.5 V, the transmitter will output correctly based on the input voltage level. In Figure 5 above the input logic level is high during power up, so the transmitter will output light.

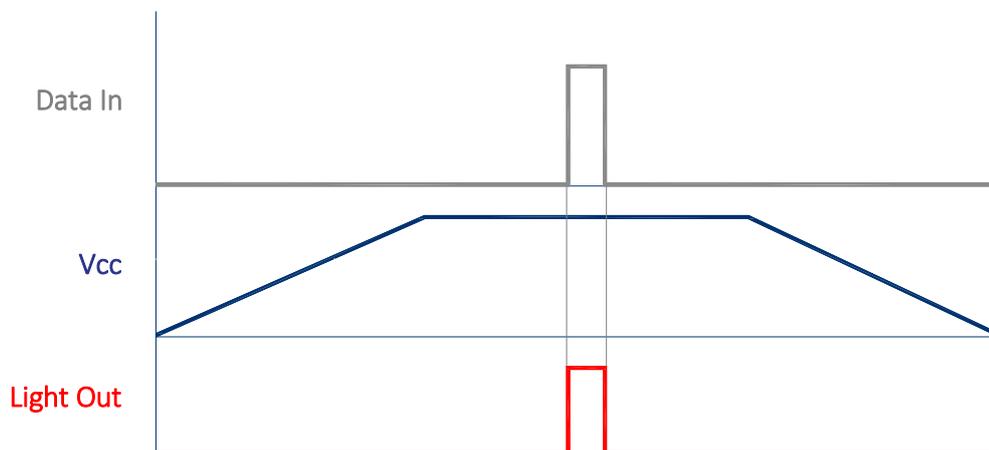


FIGURE 6
FE50MLIR Non-Inverting Tx operation during power cycling with input logic low

In Figure 6 the input logic level is low during power up, so the transmitter outputs no light.

Inverting Part FE50MLIR (Continued)

Inverting Receiver

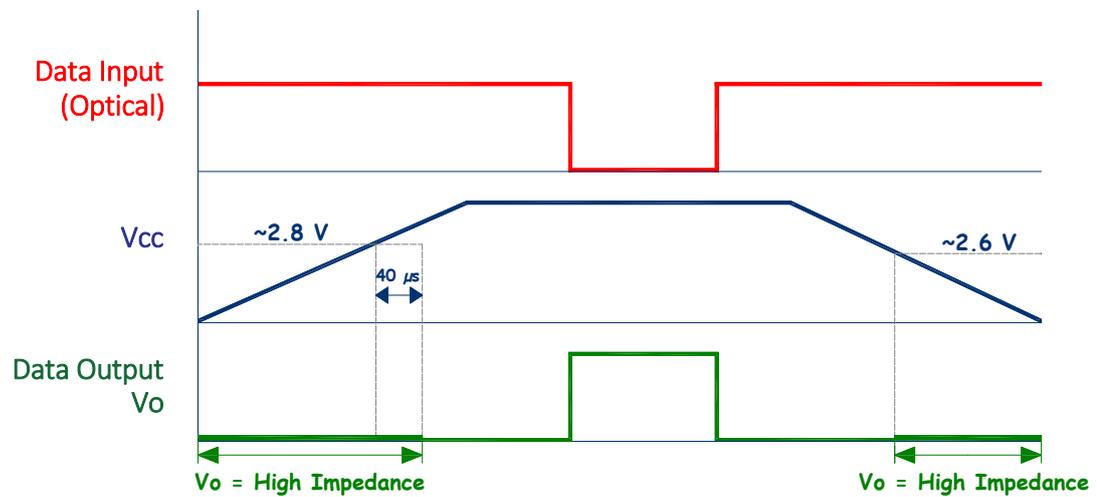


FIGURE 7
FE50MLIR Inverting Rx operation during power cycling

During power up as Vcc rises to approximately 2.8 V the output Vo is in a high impedance state. Within 40 μs of Vcc reaching 2.8 V the output Vo will change to the correct logic state which in the diagram above is logic low as there is light present and the output is inverted relative to the light input. On power down once Vcc drops below approximately 2.6 V then Vo changes immediately to a high impedance state.

Non-Inverting Part FE50MLNR

FE50MLNR consists of a non-inverting transmitter and non-inverting receiver.

Non-Inverting Transmitter

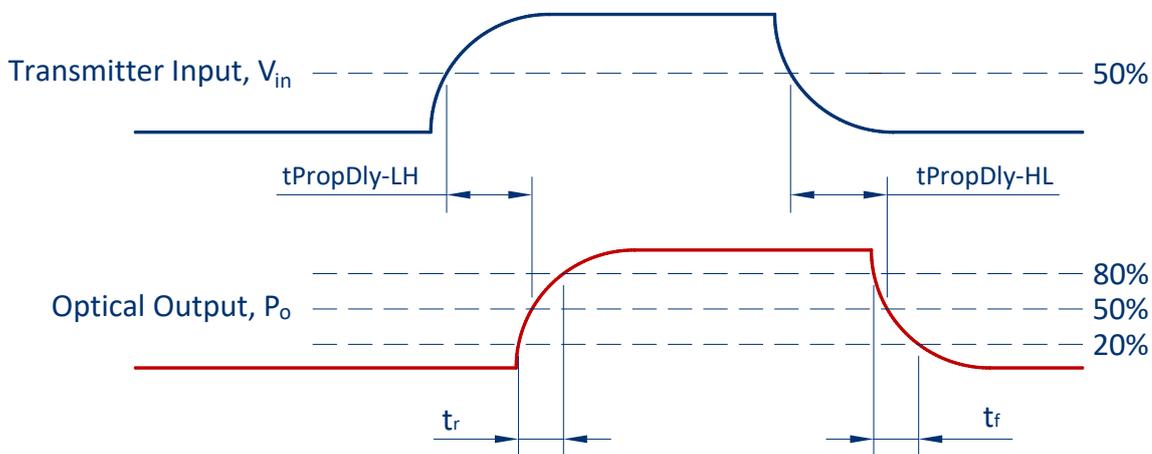


FIGURE 8
FE50MLNR Transmitter Propagation Delay and rise/fall time definitions

Non-Inverting Receiver

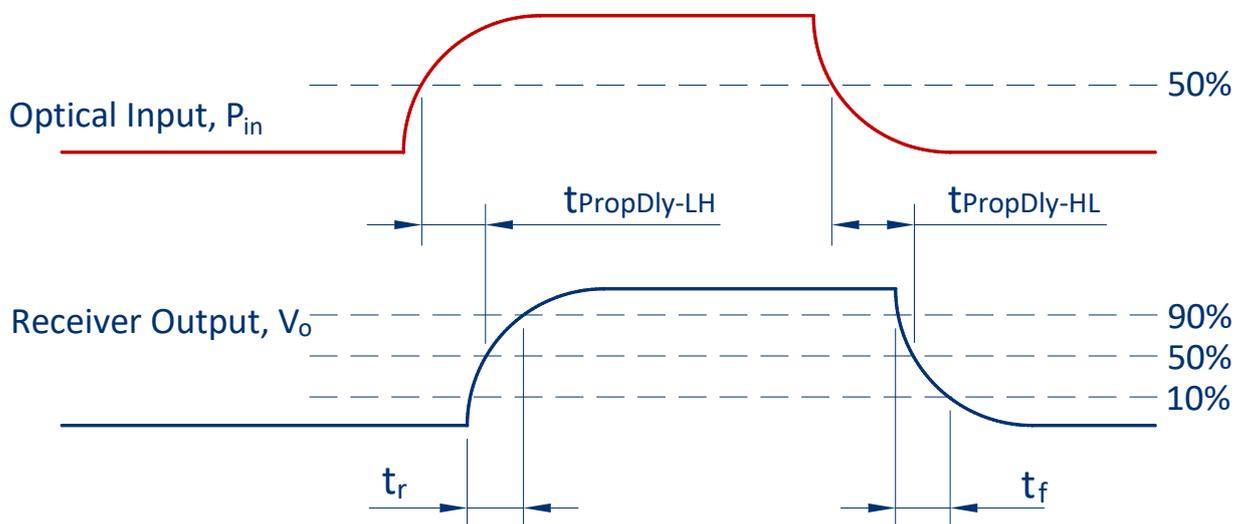


FIGURE 9
FE50MLNR Receiver Propagation Delay and rise/fall time definitions for a non-inverting V_o output

Non-Inverting Part FE50MLNR (Continued)

FE50MLNR operation during power up, power down or power reset is illustrated below in figures 10, 11 & 12.

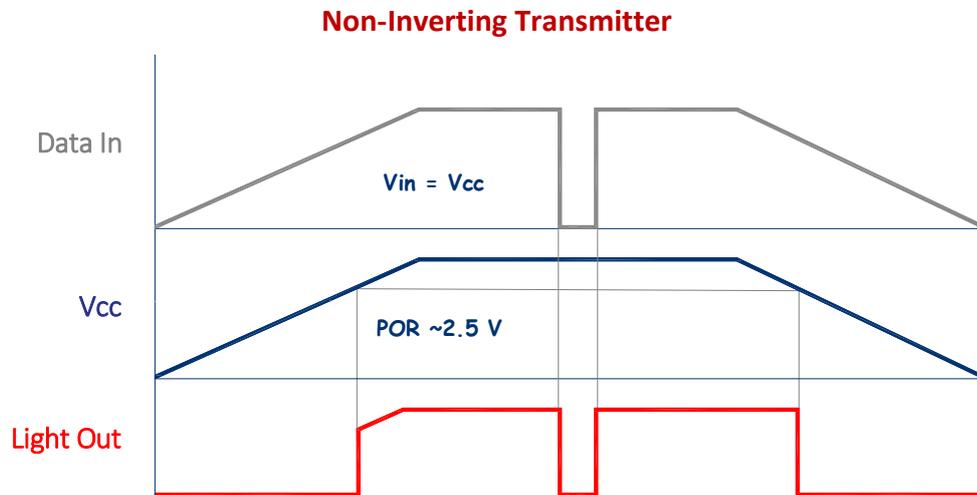


FIGURE 10
FE50MLNR Non-Inverting Tx operation during power cycling with input logic high

During power up as V_{cc} rises to approximately 2.5 V, there is no light output. Once V_{cc} reaches 2.5 V, the transmitter will output light correctly based on the input voltage level. In Figure 10 above the input logic level is high during power up, so the transmitter will output light.

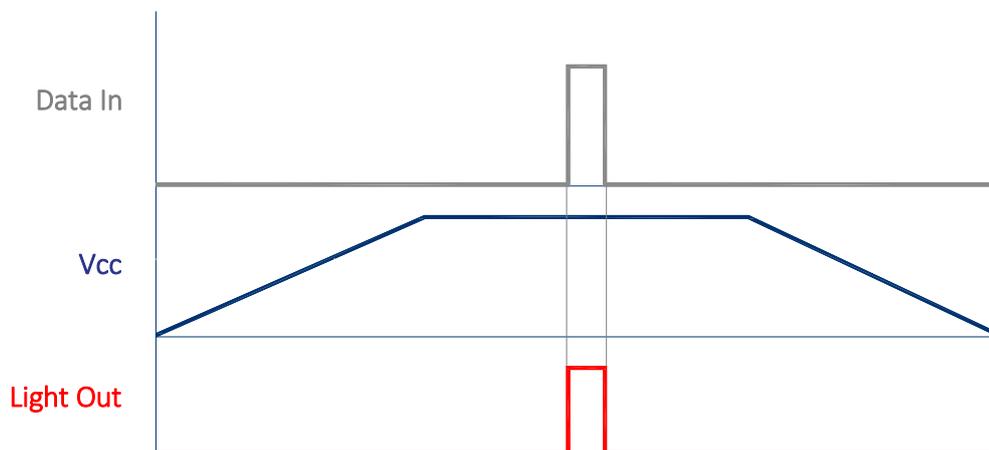


FIGURE 11
FE50MLNR Non-Inverting Tx operation during power cycling with input logic low

In Figure 11 the input logic level is low during power up, so the transmitter outputs no light.

Non-Inverting Part FE50MLNR (Continued)

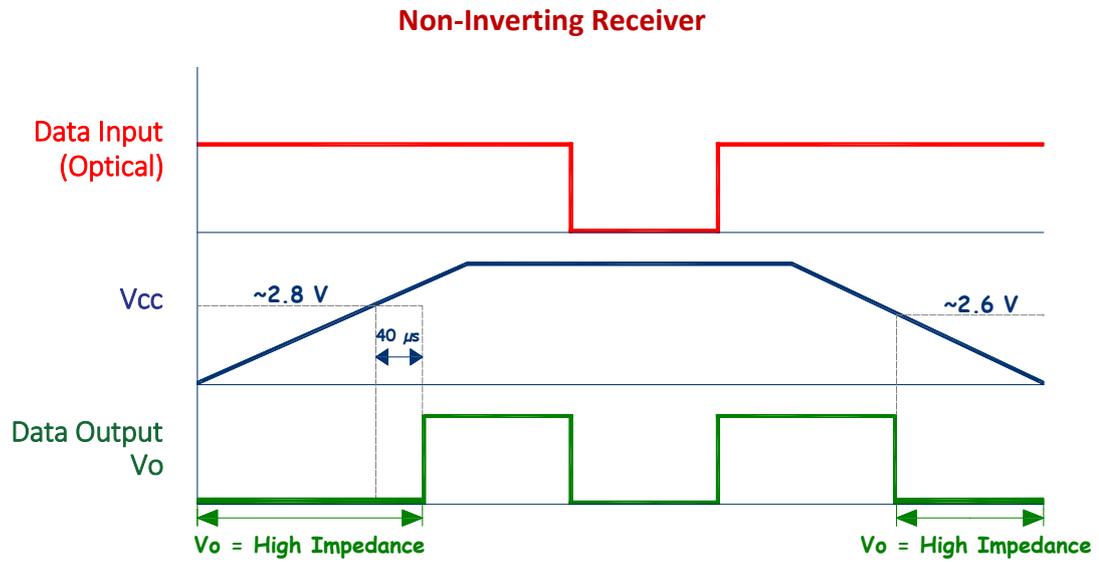


FIGURE 12
FE50MLNR Non- Inverting Rx operation during power cycling

During power up as Vcc rises to approximately 2.8 V the output Vo is in a high impedance state. Within 40 μs of Vcc reaching 2.8 V the output Vo will change to the correct logic state which in the diagram above is logic high as there is light present and the output is non-inverting. On power down once Vcc drops below approximately 2.6 V then Vo changes immediately to a high impedance state.

SPECIFICATIONS

Table 4
REGULATORY COMPLIANCE

Parameter	Symbol	Standard	Level
Electrostatic Discharge, Human Body Model (contact ESD)	HBM	JEDEC JS-001	Level 2 (2kV to < 4kV)
Storage Compliance	MSL	J-STD-020E	2a (4-week floor life)
Restriction of Hazardous Substances Directive	RoHS	Directive 2011/65/EU	Certified compliant
Eye Safety		IEC 60825-1	LED Class 1

Table 5
ABSOLUTE MAXIMUM RATINGS

These are the absolute maximum ratings at or beyond which the product can be expected to be damaged

Notes:

- 260 °C for 10 seconds, one time only, at least 2.2 mm away from lead root.*
- V_{IN} should not exceed V_{CC}. This is very important during the power-up sequence. If V_{IN} > V_{CC}, then the driver IC power from V_{IN} to power-up. This is an uncontrolled logic state and must be avoided.*

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T _{stg}	-40	+85	°C
Operating Temperature	T _{op}	-40	+85	°C
Soldering Temperature ^[1]	T _{slid}		+260	°C
Supply Voltage (TX, RX)	V _{CC}	-0.5	+5.5	V
TX Input Voltage (Data in) ^[2]	V _{IN}	-0.5	V _{CC}	V
RX Output Current	I _O	-16	+16	mA

SPECIFICATIONS

Table 6
TRANSMITTER ELECTRICAL AND OPTICAL CHARACTERISTICS

Test Conditions:

1. Test data was validated over the full temperature range of -40 °C to +85 °C, and over both power supply rail options of 5 V and 3.3 V ± 5%. Typical data out is at 25 °C, with 50 Mbps PRBS data and 3.3 V Supply.
2. Output power levels are for peak (not average) optical output levels. For 50% duty cycle data, peak optical power is twice the average optical power. Optical power is measured when coupled into 0.5 m of a 1 mm diameter 0.5 NA POF and a large area detector.
3. Electrical input pulse width is determined at 1.5 V and dV/dt between 1 V and 2 V shall not be less than 1 V/ns.
4. Emission Wavelength (centroid) $\lambda_c = \sum_i P_i \lambda_i / \sum_i P_i$. (Ref: EIA/TIA std. FOTP-127/6.1, 1991).
5. Spectral Width Root Mean Squared (RMS) $\lambda_{RMS} = (\sum_i P_i (\lambda_c - \lambda_i)^2 / \sum_i P_i)^{1/2}$. (Ref: EIA/TIA std. FOTP-127/6.3, 1991).
6. Wake Up Delay is the time from valid power up to valid data output, at 5 V or 3.3 V +/-5%, with input data at 50% duty cycle.

Parameter	Symbol	Min	Typical	Max	Unit	Test Condition
Supply Current	I _{CC}		16.5 @ 3.3 V 17.5 @ 5 V	27	mA	[1]
Input Voltage - Low	V _{IL}	-0.3		0.8	V	[1]
Input Voltage - High	V _{IH}	2		V _{CC} + 0.25	V	[1]
Data Input Capacitance	C _{in}			7	pF	
Data Input Resistance	R _{in}	10			MΩ	
Output Power	P _{High}	-9		-1	dBm	[1,2]
Emission Wavelength (centroid)	λ_c	640	650	680	nm	[4]
Spectral Width (RMS)	λ_{RMS}			30	nm	[5]
Optical Rise time (20% - 80%)	t _r		1.6	5	ns	[1]
Optical Fall time (20% - 80%)	t _f		1.3	2	ns	[1]
Propagation Delay Low-to-High	t _{PropDly_LH}	13	22	30	ns	[1], Figure 3
Propagation Delay High-to Low	t _{PropDly_HL}	13	22	30	ns	[1], Figure 3
TX Pulse Width Distortion	PWD	-3		+3	ns	[1,4]
Wake Up Delay (power up)	t _{power-on}		20		μs	[6]

SPECIFICATIONS

Table 7
RECEIVER ELECTRICAL AND OPTICAL CHARACTERISTICS

Test Conditions:

1. *Wake up Delay is the delay from VCC > 2.75 V to when the output will respond correctly to optical input. Output is held in tristate before this time.*
2. *Test data was validated using a transmitter with an emission wavelength between 635 and 680 nm with a 5ns rise and fall time, over the full temperature range of -40 °C to +85 °C, over both supply rail voltage options of 5 V and 3.3 V ± 5%, and over the input optical received power as specified by P_H and P_L. Input power levels are for peak (not average) optical input levels. For 50% duty cycle data, peak optical power is twice the average optical power. Data referred to as typical are rated at +25 °C.*
3. *Optical signal from the recommended Transmitter circuit.*
4. *Testing in the recommended receiver circuit (RL= 50 kΩ, CL(total)= 15 pF).*
5. *PWD for Optical Input of 50 MBd, NRZ 27-1 (PRBS7) data, resulting in a BER ≤ 10⁻⁹.*
6. *PWD for 1st to 3rd pulse is characterized with minimum Optical Input pulse width of 20 ns, with the 1st pulse being the worst case. For pulses > 20 ns the PWD will be less. If data rate < 1 MBd, then the pulse width distortion = PWD 1st to 3rd pulse.*
7. *The performance of the receiver as given in Table 7 has been characterized for transmitters operating between 635 and 680 nm. The receiver will nevertheless respond to optical sources operating from the visible to near infra-red regions although the precise performance may differ from that given in Table 7 depending upon the precise wavelength and rise/fall time characteristics of the optical source used.*

Parameter	Symbol	Min	Typical	Max	Unit	Test Condition
Supply Current	I _{CC}		20	25	mA	[2,3,4]
Wake Up Delay (power up)	t _{power-on}		40		μs	[1]
High Level Output Voltage	V _{OH}	V _{CC} – 0.05		V _{CC}	V	I _{OH-max} = 40 uA, [2]
Low Level Output Voltage	V _{OL}	0		0.05	V	I _{OL-max} = 1.6 mA, [2]
Optical Power High	P _H	-22		-1	dBm	[2,3]
Optical Power Low	P _L			-40	dBm	[2,3]
Data Rate		DC		50	MBd	Min UI = 20 ns, Max f = 25 MHz
Output Rise Time (10% - 90%)	t _r			6	ns	[2,3,4]
Output Fall Time (10% - 90%)	t _f			6	ns	[2,3,4]
Pulse Width Distortion for PH range -20 to + 2 dBm	PWD	-4		4	ns	[2,3,4,5]
Pulse Width Distortion for PH range -20 to -22 dBm	PWD	-6		6	ns	[2,3,4,5]
Pulse Width Distortion 1st to 3rd pulse	PWD _{init}	-7		14	ns	[2,3,4,5,6]
Propagation Delay	t _{PropDly-HL}			50	ns	[2,3,4]
	t _{PropDly-LH}			50	ns	[2,3,4]
Optical Sensitivity Range	λ _R	400		900	nm	[7]

MECHANICAL DATA

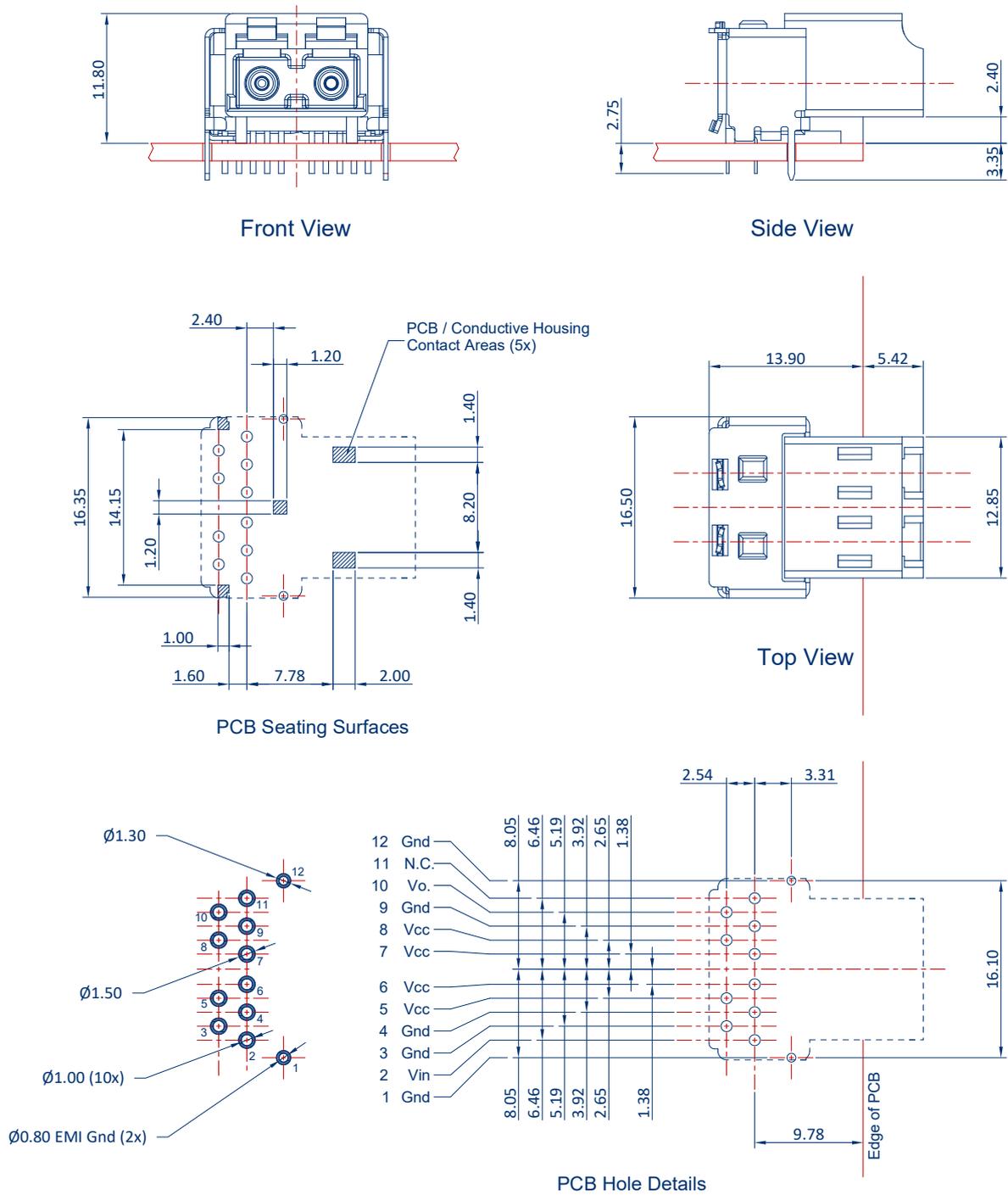


FIGURE 13
 Mechanical dimensions of the product, and PCB footprint, which is a top view
 General dimensional tolerance is ± 0.2 mm

Note: The plastic housing of the FE50MLIR/FE50MLNR LC connector is made from an electrically conductive fibre-filled plastic material. Electrically conductive traces on the connector seating surface of the printed circuit board should not run underneath the connector housing. If it is necessary to run electrically conductive traces underneath the connector, their positions must not coincide with the PCB seating surfaces shown above.

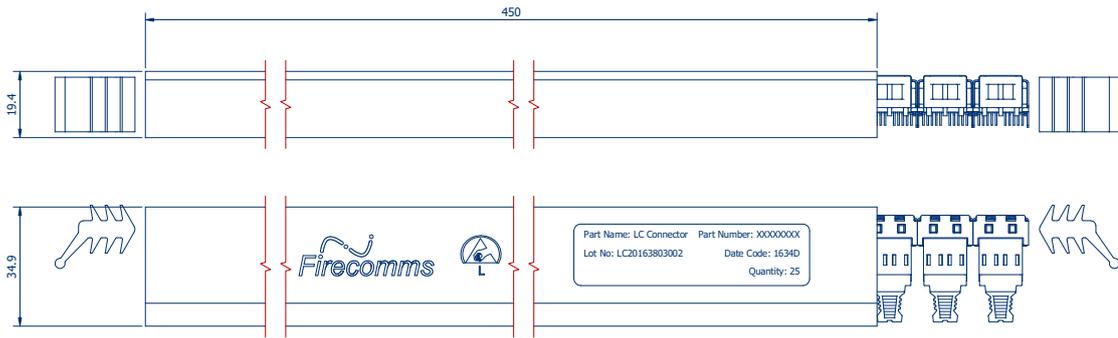


FIGURE 14
Packing tube for Firecomms FE50MLIR FE50MLNR LC Transceivers

PART HANDLING

The transceivers are tested for handling in static-controlled assembly processes (HBM). Cleaning, degreasing and post solder washing should be carried out using standard solutions compatible with both plastics and the environment. For example, recommended solutions for degreasing are alcohols (methyl, isopropyl and isobutyl). Acetone, ethyl acetate, phenol or similar solution based products are not permitted.

In the soldering process, non-halogenated water soluble fluxes are recommended. These connectors are not suitable for use in reflow solder processes (infrared/vapor-phase reflow). The dust plug should remain in place during soldering, washing and drying processes to avoid contamination of the active optical area of each connector.

The Moisture Sensitivity Level (MSL) classification of this device is 2a according to JEDEC J-STD-020E. The shelf life of an unopened MBB (Moisture Barrier Bag) is 24 months at < 40 °C and < 90 % R.H. Once the Moisture Barrier Bag is opened the devices can be either

- a) Stored in normal factory conditions < 30 °C and < 60 % R.H. for a maximum of 672 hours (4 Weeks) prior to soldering.
- b) Stored at < 10 % R.H. (Dry Cabinet).

PACKING INFORMATION

Components are packed in PVC anti-static tubes in moisture barrier bags. Bags should be opened only in static-controlled locations, and standard procedures should be followed for handling moisture sensitive components.

Components per Tube	25
Tube Length	450 mm
Tube Width	34.9 mm
Tube Height	19.4 mm
Tubes per Bag	10
Bags per Inner Carton	1
Inner Carton Length	588 mm
Inner Carton Width	147 mm
Inner Carton Height	82 mm
Weight per Inner Carton, Complete	1.95 kg
Components per Inner Carton	250
Inner Cartons per Outer Carton	4
Outer Carton Length	600 mm
Outer Carton Width	310 mm
Outer Carton Height	195 mm
Weight per Outer Carton, Complete	8.10 kg
Components per Outer Carton	1,000

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